Ku-Band 15W Single-Chip HJFET Power Amplifier

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ABSTRACT

This paper describes record power performance of Ku-band power amplifiers fabricated with a 0.45 μm gate GaAs-based heterojunction FET (HJFET). The developed HJFET amplifier with 25.2mm gate periphery delivered a 41.98dBm (15.8W) output power with 36% power-added efficiency (PAE) and 9.6dB linear gain at 12GHz. This is the highest PAE, gain and output power combination achieved from a single-chip FET power amplifier at Ku-band.

INTRODUCTION

There is growing demand for solid state power amplifiers (SSPAs) capable of delivering increased output power with reasonable efficiency. A GaAs-based heterojunction FET (HJFET) has emerged as a viable candidate for high-efficiency power devices at microwave frequencies. The HJFET device has demonstrated excellent performance of high output power, gain and PAE, making it attractive for various SSPA applications. This is due to its inherent high drain current and high gain characteristics along with its high gate breakdown voltages.

To date, GaAs-based single-chip FETs with large-periphery have already demonstrated impressive power performances. These include an output power of 6W and 50% PAE with 8mm gate-width at 12GHz[1-2], 11.2W and 41% PAE with 23.1mm at12GHz[3], and 10.9W and 32% PAE with 19.2mm at 14GHz[4]. We have also reported a large periphery 16.8mmHJFET power amplifier demonstrating 10W level at 12GHz[5-6]. In order to further improve the output power under high PAE, development of single-chip HJFETs with larger gate periphery is strongly required.

In this paper, an internally-matched single-chip HJFET amplifier is described with record power performance at Ku-band.

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DEVICE CHARACTERISTICS

The cross-section of the device structure is shown in Fig.1. Step-recessed 0.45 μm gate-length HJFETs were fabricated on a 3-inch GaAs substrate. The active part of the MBE-grown HJFET structure consists of a 13nm undoped $In_{0.2}Ga_{0.8}As$ channel layer sandwiched between two Si-doped $Al_{0.22}Ga_{0.78}As$ layers. The doping densities for the upper (8nm) and the lower (4nm) AlGaAs donor layers are 4.5×10^{18} cm^{-3} and $4\times10^{18}cm^{-3}$, respectively. To achieve high gate-to-drain breakdown voltage (BV_{gd}) while maintaining high maximum drain current (I_{max}), an n^+/n^- dual cap layer and an undoped AlGaAs Schottky layer were employed. The wafer processing began with first wide recess formation, followed by a standard NiAuGe metallization for source and drain Ohmic contacts. The narrow recess was then formed using wet chemical etching to a desired current level. WSi metal was sputter-deposited onto a recessed undoped AlGaAs Schottky layer to form a 0.45 μm T-shaped gate. The wide recess width

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was 2.0 μm. The devices were passivated with a plasma-enhanced CVD silicon-nitride film. The wafer was then thinned to 30 μm. Slot via-holes were etched underneath the source pad, and the flip-side of the wafer was plated with 20 μm thick gold to ensure low thermal resistance.

The device exhibited an I_{max} of 510mA/mm with a drain saturation current (I_{dss}) of 240mA/mm. I_{max} was defined at a gate bias of +1V. The device exhibited a maximum transconductance of 400mS/mm, a BV_{gd} of more than 18V and a pinch-off voltage of -0.6V.

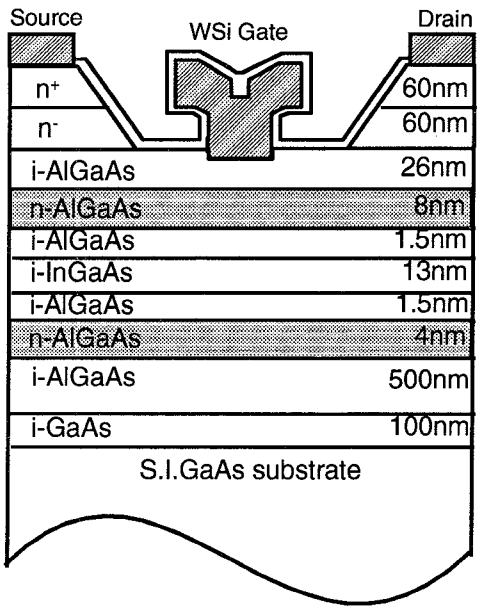

Fig.1. Cross section of the 0.45 μm gate-length step-recessed HJFET.

AMPLIFIER CIRCUIT DESIGN

It is well known that as the unit gate width increases, device gain decreases due to the increase in the gate resistance and phase mismatches. Figure 2 shows Maximum Unilateral Gain (MUG) evaluated at 12GHz as a function of the gate width. The device was biased at a drain bias voltage (V_d) of 9V with a drain current of $1/2I_{dss}$. When the unit gate width was increased to beyond 200 μm, significant reduction in MUG was observed. However, MUG degradation at 12 GHz was found to be suppressed within 0.2dB up to the gate width of 150 μm. Therefore, the unit gate width of a single-chip 25.2mm power HJFET was chosen to be 150 μm so as to suppress the increase in the total cell number of 12, which was employed for a 16.8mm HJFET (with unit gate width of 100 μm) previously reported[6].

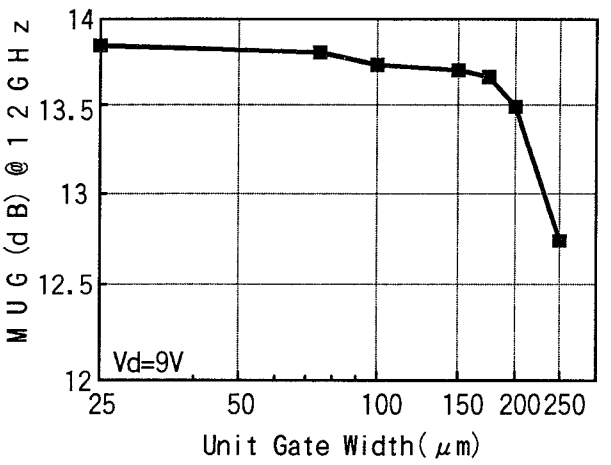

Fig.2. Measured MUG as a function of unit gate width at 9V.

The amplifier circuit design procedure was almost the same as that previously reported[5-6]. The output matching circuit was designed using a large-signal load impedance determined from load-pull measurements performed on a 1mm HJFET. The measured large-signal load impedance was then scaled to model a 25.2mm HJFET.

The input and output matching circuits were composed of L-C-L section transformers, quarter wave transformers and low-impedance transmission lines. The input matching circuit was designed to achieve maximum gain by considering the small-signal equivalent circuit of the 25.2mm HJFET. The low-impedance transmission lines were used to reduce circuit loss.

Figure 3 shows a photograph of the developed internally matched HJFET power amplifier. The L-C-L section transformer consists of a Metal-Insulator-Metal capacitor with 150 μm thick Barium Titanate and bonding wire inductors. The quarter wave transformer and low-impedance transmission lines were formed on a 250 μm thick alumina substrate. The package size of the power amplifier, excluding the bias lines, was $16.5\times9.7mm^2$ with an actual circuit size of $5.0\times7.5mm^2$.

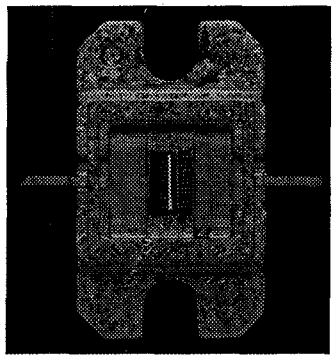

Fig.3. Photograph of internally matched HJFET amplifier.

AMPLIFIER PERFORMANCE

The power amplifier was mounted on a specially designed waveguide test fixture for evaluation of gain, return loss and large-signal power characteristics. The fixture input and output losses of 0.25dB were measured and removed from all measurement results.

Figure 4 shows the measured small signal gain, input and output return losses of the power amplifier as a function of frequency. The small signal gain was 9.6dB at 12GHz with V_d=9V. The input and output return losses were less than -25dB and -23dB, respectively.

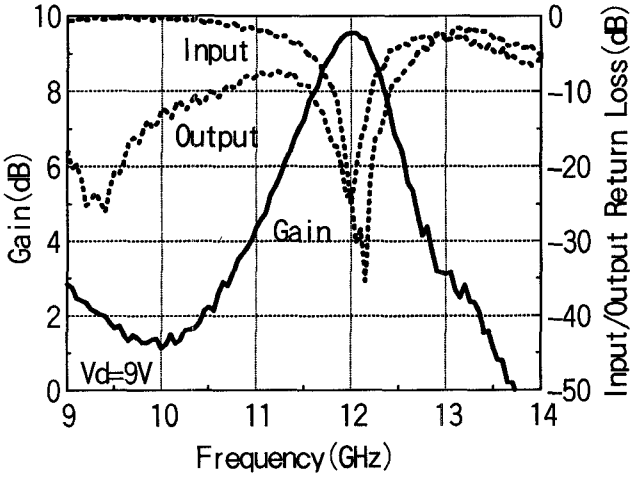

Fig.4. Measured small signal response of power amplifier. V_d=9V.

The power characteristics measured under C.W. operating conditions are shown in Fig.5. At 12GHz, the fabricated power amplifier demonstrated an output power of 41.5dBm (14.1W) with 9.8dB linear gain and 41% PAE at V_d=8V. At V_d=9V, it delivered 41.98dBm (15.8W) output power with 9.6dB linear gain and 36% PAE. To the authors' knowledge, this is the highest output power ever achieved from a single FET power amplifier at this frequency. At 2dB gain compression operation point, 41.39dBm (13.8W) output power and 31% PAE were obtained at V_d=9V.

The frequency dependence of the power characteristics are shown in Fig.6. Over the 11.8-12.2GHz frequency range, the amplifier exhibited 13.9-15.3W output power with PAE of 33-34% with V_d=9V and an input power of 35dBm.

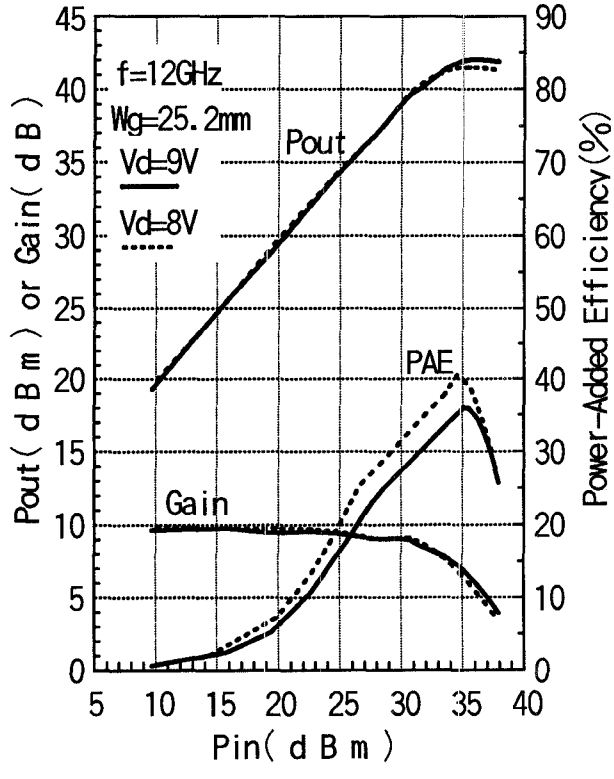

Fig.5. Measured output power, gain and power-added efficiency as a function of input power at 12GHz for internally matched 25.2mm HJFET power amplifier. V_d=8 and 9V.

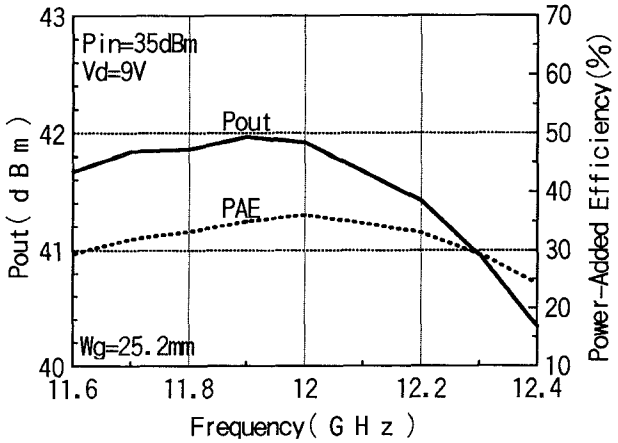

Fig.6. Measured frequency response of 25.2mm HJFET amplifier 11.6-12.4GHz band.

Power performance of the single-chip FET amplifier developed in this work is plotted in Fig.7, together with the previous results reported at X-Ku band[3-4]. The higher gain characteristics of the developed HJFET amplifiers are responsible for the superior PAE achieved under over 10W operating conditions.

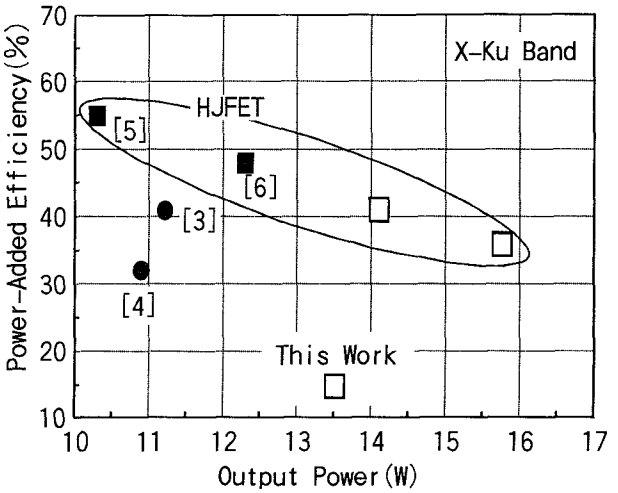

Fig.7. Power performance of single-chip FETs at X-Ku band.

CONCLUSIONS

High output power amplifier fabricated with a single-chip HJFET was demonstrated at Ku-band. It was found that the gain degradation at 12GHz due to increased unit gate width is less than 0.2dB up to the gate width of 150 μ m. The developed HJFET amplifier with 25.2mm gate periphery delivered a 41.98dBm (15.8W) output power with 36% power-added efficiency and 9.6dB linear gain at 12GHz. To the authors' knowledge, this is the highest output power ever achieved from a single-chip FET power amplifier at this frequency.

The present power HJFET technology is promising for various satellite communication and radar system applications.

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